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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/617,834	07/14/2003	Koji Wakayama	H-1100	5217

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EXAMINER	
WONG, XAVIER S	
ART UNIT	PAPER NUMBER
2416	
MAIL DATE	DELIVERY MODE
04/28/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/617,834	WAKAYAMA ET AL.	
	Examiner	Art Unit	
	Xavier Szewai Wong	2416	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *9th April 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-8 and 10-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-8 and 10-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 9th April 2009 has been entered.

Claim Objections

Claims 4-8, 10, 11 and 13-15 are objected to because of the following informalities: change "according to **C**laim" into small letters, e.g. -- according to claim 1 --.

Claim 1 is objected to because of the following informalities: line *1* – consider delete "of" (An apparatus of...) and insert -- for --.

Claim 8 is objected to because of the following informalities: line *3* – delete "processor" and insert -- processor*s* --.

Claim 12 is objected to because of the following informalities: line *1* – consider delete "of" (A method of...) and insert -- for --.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Badamo et al (US 2002/0181476 A1, Badamo) in view of Pham et al (US 7283538 B2, Pham).

Claims 1, 4, 8 and 12: Badamo shows an apparatus and method for transmitting packets (fig. 3; [0035]: hardware architecture), comprising:

a plurality of line cards which have interfaces for transmitting and receiving packets (fig. 3: LC-1~8);

switches connected to said plurality of line cards (fig. 3: FC(s) switch fabric);

a plurality of extension function processors connected to said switches (fig. 3: SC-1~6), the extension function processors performing processing to be executed on a higher layer than a layer on which a received packet is transferred ([0036] lines 6-7: LCs handle PHY and MAC layer functions; [0036] lines 9-10: SCs handle forwarding path and protocol stacks → [0046] lines 5-15: SC performs encryption – encryption is performed in the extension function processors → higher layer processing: as described in applicant specification pg. *13* lines *11-13*; [0048] lines 3-13: NAT = layer 3 process).

Yet, Badamo does not very expressively mention: "a statistic information collecting processor connected to said switches, said statistic information collecting processor including means for analyzing header information imparted to said packets, and means for counting an amount of packets to be transmitted or received through said interfaces,

wherein said statistic information collecting processor predicts the amount of packets to be received by said plurality of interfaces from said header information and said amount of packets which have been analyzed, and

wherein on the basis of said predicted amount of packets received by all of the line cards, an extension function processor to which packets are transmitted is selected from the extension function processors and implements processing on the packets so as to allocate to each extension function processor uniformly an amount of traffic that is processed in each extension function processor."

Pham teaches a statistic information collecting processor (fig. 4: control processor 84 or crypto processor 86) connected to said switches (fig. 4: crossbar 78), said statistic information collecting processor including means for analyzing header information imparted to said packets (col. 14 lines 35-37: header is examined), and means for counting an amount of packets to be transmitted or received through said interfaces (col. 13 lines 66-67: quantitative data… of data packets),

wherein said statistic information collecting processor predicts the amount of packets to be received by said plurality of interfaces from said header information and said amount of packets which have been analyzed (col. 13 line 61 – col. 14 line 4: predictive selection… implement effective load balanced distribution of network data packets to the crypto processors), and

wherein on the basis of said predicted amount of packets received by all of the line cards (col. 10 lines 25-32: load-balancing algorithm is optimized to *account for full processing path of data packets* through the gateway), an extension function processor to which packets are transmitted is selected from the extension function processors and implements processing on the packets so as to allocate to each extension function processor uniformly an amount of traffic that is processed in each extension function

processor (col. 10 lines 32-42: account for differences in performance capabilities of the crypto processors… load-balancing; col. 13 line 57 – col. 14 line 4: ingress processor checks availability of crypto processors and selects a crypto processor for load-balancing (e.g. uniform) distribution of data packets).

It would have been obvious to one of ordinary skill in the art when the invention was created to modify the extension function processors (fig. 3: SCs) and control processor (fig. 3: CC) of Badamo to comprise of the statistic information collection functions as mentioned by Pham for load-balancing of the processors.

Claim 4: Badamo, in combination with Pham, shows a bus for directly connecting said interfaces and said statistic information collecting processor (fig. 3: PCI bus 34/38 connect SCs and LCs through CC).

Claim 8: Badamo teaches the claimed invention; yet "a plurality of [said] statistic information collecting processors" is not expressively mentioned. Pham shows a plurality of statistic information collecting processors (fig. 4: control processor 84 or crypto processor 86; col. 13 lines 66-67: quantitative data… of data packets). It would have been obvious to one of ordinary skill in the art when the invention was created to implement the plurality of statistic information collecting processors as taught by Pham to the apparatus of Badamo to allow efficient calculation of load among the extension function processors for load balancing.

Claims 5, 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Badamo et al (US 2002/0181476 A1, Badamo) in view of Pham et al (US 7283538 B2, Pham), applied to claim 1, and in further view of Fukumoto et al (US 2003/0012139 A1, Fukumoto).

Claim 5: Badamo, in combination with Pham, teaches the interfaces for transmitting and receiving packets; yet the specifics of "have means for storing, in a frame, at least a portion of plural headers imparted to a plurality of packets which said interfaces transmit and receive, and means for transmitting the frame to the statistic information collecting processor" are not expressively mentioned. Fukumoto teaches have means for storing, in a frame, at least a portion of plural headers imparted to a plurality of packets which said interfaces transmit and receive ([0040]: header extraction section memory; fig. *2* items *12* & *19*; fig. *11* S*14*: IP header extracted), and means for transmitting the frame to the statistic information collecting processor ([0042]: e.g. counter and flow identification; claim *1*; fig. *2* items *16* & *17*). It would have been obvious to one of ordinary skill in the art when the invention was created to modify the line card interfaces of Badamo, in combination with Pham, to explicitly include means for header storing and means for transmitting the frame to the statistic processor as taught by Fukumoto for effective monitoring of amount of traffic in a network [0008].

Claim 10: Badamo, in combination with Pham, discloses the claimed invention; yet "a table provided in each of said line cards, on which a relationship of header information corresponding to amount of received packets and an output line card of the packet is described, and a statistics table provided in said statistic information collecting

processor, on which is described a relationship of a correspondence between header information of the received packets and said amount of packets" are not very expressively mentioned. Fukumoto et al disclose a table provided in each of said line cards, on which a relationship of header information corresponding to amount of received packets and an output line card of the packet is described (a plurality of line cards *each* comprising a switch interface section and counter section and a function to monitor the amount of received packets during communication and determine an outgoing path with reference to information header (shows) through memory#1 and memory#0 of received IP packets in [*0037-38* & *0040-42*]; *abstract*; claim *1*), and a statistics table provided in said statistic information collecting processor, on which is described a relationship of a correspondence between header information of the received packets and said amount of packets (memory#1 and memory#0 show each line cards and therefore; showing a relationship of a correspondence between header information and an output line card [through the destination port] in [*0040-41* & *0053*]; fig. *1* port ↔ line card links; fig. *9*). It would have been obvious to one of ordinary skill in the art when the invention was created to modify the line cards and statistic information collecting processor(s) of Badamo, in combination with Pham, to quickly account for traffic load in each line interface and thus, effectively adjust load in each processor.

Claim 11: Badamo, in combination with Pham, discloses the claimed invention; yet "means for renewing said table provided on each of said line cards on the basis of said amount of packets predicted" is not specifically mentioned. Fukumoto teaches means for renewing said table provided on each of said line cards on the basis of said amount of packets predicted ([0042]: counter section and memory *controls* a packet counter).

It would have been obvious to one of ordinary skill in the art when the invention was created to include means for renewing the statistics table as taught by Fukumoto to the statistics information collecting processor of Badamo, in combination with Pham, since packet number prediction varies from time to time and dynamic accountability is needed to adjust load balance among the processors.

Claims 6, 7, 13, 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Badamo et al (US 2002/0181476 A1, Badamo) in view of Pham et al (US 7283538 B2, Pham), as applied to claims 5, 12 and 13, and in further view of Shiota (US 6987762 B2).

Claims 6 and 13: Badamo, in combination with Pham, discloses the claimed invention above; yet does not *specifically* mention the headers that are to be multiplexed into a frame and are all equal to one another in size. Shiota discloses the headers that are to be multiplexed into a frame and are all equal to one another in size (SHIM headers stored in a frame are attached (multiplexed) into the frame and are all equal to one another in size in figs. *12* & *13*; col. *13* ln. *30-51*). It would have been obvious to one of ordinary skill in the art to incorporate the teachings of an apparatus that attaches (multiplexes) headers of equal sizes as taught by Shiota in the apparatus of Badamo, in combination with Pham, to identify packet destinations in a sequenced fashion.

Claim 7: Badamo, in combination with Pham, discloses the claimed invention above; yet not *specifically* mention means for multiplexing determines length of a header portion to be extracted from a plurality of packets in response to information

indicating classification of the packets and that the packets are to be multiplexed into one frame. Shiota discloses (SHIM) headers stored in a frame are attached (multiplexed) into the frame and are all equal to one another in size and further teaches the classification of packets and headers into one frame (figs. *2* (item *15*), *12* & *13*; col. *9* ln. *13-29*; col. *13* ln. *30-61*). It would have been obvious to one of ordinary skill in the art to incorporate the teachings of an apparatus that attaches (multiplexes) headers of equal sizes and classifying headers and packets as taught by Shiota in the apparatus of Badamo, in combination with Pham, to identify packet destinations for each of the packets in sequence.

Claim 14: Badamo, in combination with Pham, discloses the claimed invention; yet "extracting only a portion of said headers corresponding to a fixed length from said received packets" is not specifically mentioned. Shiota teaches extracting only a portion of said headers corresponding to a fixed length from said received packets (fig. 12: SHIM headers of the same size; col. 13 lines 33-55: label process based on classification). It would have been obvious to one of ordinary skill in the art when the invention was created to implement function of extracting only a portion of a header corresponding to a fixed length as taught by Shiota to the header extracting process of Badamo, in combination with Pham, since only the classification info is needed for forwarding and reduces overhead.

Claim 15: Badamo, in combination with Pham, disclose the claimed invention except specifically mentioning extracting a header of the received packet only by a size corresponding to information indicating classification of the packet set to a header to be

imparted to each of the packets. Shiota discloses extracting a header of a received packet (col. *13* ln. *30-40*) only by a size corresponding to classification of the packet set to a header to be imparted to each of the packets (col. *13* ln. *45-55*; e.g. shim header length). It would have been obvious to one of ordinary skill in the art to incorporate the function of classifying headers as taught by Shiota in the apparatus of Badamo, in combination with Pham, for rapid MPLS and IP processing.

Response to Arguments

Applicant's arguments with respect to amended claims 1 and 12 have been considered but are moot in view of the new ground(s) of rejection by new reference.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. Yu, US 6078943: a statistics collector to acquire load info from a cluster of servers for reporting to achieve load balance among the servers

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Xavier Wong whose telephone number is 571.270.1780. The examiner can normally be reached on Monday through Friday 8:30 am - 6:00 pm (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema Rao can be reached on 571.272.3174. The fax phone number for the organization where this application or proceeding is assigned is 571.273.8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866.217.9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800.786.9199 (IN USA OR CANADA) or 571.272.1000.

/Xavier Szewai Wong/
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23rd April 2009

/Kevin C. Harper/
Primary Examiner, Art Unit 2416